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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/830,515	08/03/2001	Ryoji Suzuki	SON-1885/SUG	8204

23353 7590 05/04/2005

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EXAMINER	
QUIETT, CARRAMAH J	
ART UNIT	**PAPER NUMBER**
2612	

DATE MAILED: 05/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/830,515	SUZUKI ET AL.	
	Examiner	Art Unit	
	Carramah J. Quiett	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 9-13* is/are rejected.

7)☒ Claim(s) *7-8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *8/03/01* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/27/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement (IDS), filed on 04/27/2001, has been placed in the application file, and the information referred to therein has been considered as to the merits.

Drawings

3. Figure 13 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

4. **Claim 7** is objected to because of the following informalities:

In regards to claim 7, this claim has been submitted by the Applicant stating, "A solid-state image pickup device as claimed in *claim 1*, wherein *said vertical drive means* successively output the pixel signals to said vertical line via said horizontal signal line, *said horizontal drive means* feeds a horizontal selection pulse to *said read out selection transistor* and *said output selection transistor*." Please note that "said read out selection transistor and said output selection transistor" are not claimed in claim 1. It is more appropriate for claim 7 to be dependent on claim 6 instead. Therefore, the Examiner will treat claim 7 as being dependent on claim 6. Additionally, limitations such as "said vertical drive means" and "said horizontal drive means" are not mentioned in claim 1 (nor claim 6). Instead, those limitations should be written as "said vertical driving means" and "said horizontal driving means." Respectfully, the wording in each claim must be consistent. Please correct these errors and other errors similar to these in other claims as well. Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. **Claims 1 and 3** are rejected under 35 U.S.C. 102(e) as being anticipated by Yadid-Pecht et al. (#6,115,065).

For **claim 1**, Yadid-Pecht discloses a solid-state image pickup device (in figs. 2-3) comprising:

- a pixel portion (fig. 2, ref. 202) in which unit pixels are arranged in a matrix form (col. 4, lines 41-57);
- horizontal signal lines of plural rows which are wired to said pixel portion on a row basis (col. 4, lines 59-65);
- plural vertical signal lines which are wired commonly to said horizontal-signal lines of plural rows (col. 4, lines 59-65);
- vertical driving means of plural systems (col. 4, lines 59-65) which select the respective pixels of said pixel portion every row over plural different rows (col. 5, lines 18-21 and 40-43), making the accumulation time of signal charges of each pixel of the plural selected rows different among the plural rows (col. 5, lines 22-31 and 47-50), and successively outputting to said plural vertical signal lines the signals which are output from the respective pixels to said horizontal signal lines of plural rows (col. 5, lines 31-36); and
- horizontal driving means for successively selecting the pixels of plural rows which are selected by said plural systems of vertical driving means (col. 4, lines 59-65).

As for **claim 3**, Yadid-Pecht discloses a method of driving a solid-state image pickup device (in figs. 2-3) comprising a pixel portion (fig. 2, ref. 202) in which unit pixels are arranged in a matrix form (col. 4, lines 41-57), horizontal signal lines of plural rows which are wired to said pixel portion on a row basis (col. 4, lines 59-65), and plural vertical signal lines which are wired commonly to the horizontal signal lines of plural rows (col. 4, lines 59-65), characterized by the steps of:

- selecting the respective pixels of the pixel portion every row over plural different rows (col. 5, lines 18-21 and 40-43);
- making the accumulation time of signal charges of each pixel of the plural selected rows different among the plural rows (col. 5, lines 22-31 and 47-50);
- successively selecting the respective pixels of plural rows thus selected and outputting the signal of each pixel to the corresponding one of the horizontal signal lines of plural rows (col. 5, lines 31-36); and
- outputting through the plural vertical signal lines the signals which are output from the respective pixels to the horizontal signal lines (col. 4, lines 49-51 and 59-65; col. 5, lines 31-36).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. **Claim 2** is rejected under 35 U.S.C. 103(a) as being unpatentable over Yadid-Pecht et al. (#6,115,065) in view of Todaka et al. (#4,835,617).

For **claim 2**, Yadid-Pecht teaches a solid-state image pickup device wherein a control circuit has row and column decoders for addressing the proper row/column of pixels, clock generator circuits for synchronization, and readout circuits. The control circuit is operable to control the readout of the pixels and the operation of the column-parallel signal chain(s) in a desired sequence with desired integration time(s). Please read col. 4, lines 59-65. However, Yadid-Pecht does not expressly disclose a solid-state image pickup device wherein said vertical driving means of plural systems has vertical selection switches of plural systems which are connected between each of said horizontal signal lines of plural rows and said plural vertical signal lines, and plural vertical scan circuits which are provided in connection with said vertical selection switches of plural systems and successively drive said vertical selection switches of different rows by a vertical scan operation.

In the same field of endeavor, Todaka discloses a solid-state image pickup device (figs. 1, 3, and 4) comprising vertical driving means (fig. 1, 4; col. 3, lines 3-25) of plural systems has vertical selection switches (137/138) of plural systems which are connected between each of said horizontal signal lines (133) of plural rows (OY_1/OY_2) and said plural vertical signal lines (135), and plural vertical scan circuits (111/211) which are provided in connection with said vertical selection switches of plural systems and successively drive said vertical selection switches of

different rows by a vertical scan operation (col. 4, lines 9-43). In light of the teaching of Todaka, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yadid-Pecht's solid-state image pickup device with a vertical driving means of plural systems has vertical selection switches of plural systems which are connected between each of horizontal signal lines of plural rows and plural vertical signal lines, and plural vertical scan circuits which are provided in connection with the vertical selection switches of plural systems and successively drive the vertical selection switches of different rows by a vertical scan operation. This procedure allows the charges in two horizontal lines of an image sensor to be read simultaneously therefore preventing the occurrence of image deterioration and flicker (Todaka, col. 1, lines 59-64).

10. **Claims 4-5** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yadid-Pecht et al. (#6,115,065).

For **claim 4**, Yadid-Pecht discloses a solid-state image pickup device a solid-state image pickup device comprising: a pixel portion (fig. 2, ref. 202) in which unit pixels are arranged in a matrix form (col. 4, lines 41-57); horizontal signal lines of plural rows which are wired to said pixel portion on a row basis (col. 4, lines 59-65); plural vertical signal lines which are wired commonly to said horizontal-signal lines of plural rows (col. 4, lines 59-65); vertical driving means of plural systems (col. 4, lines 59-65) which select the respective pixels of said pixel portion every row over plural different rows (col. 5, lines 18-21 and 40-43), making the accumulation time of signal charges of each pixel of the plural selected rows different among the plural rows (col. 5, lines 22-31 and 47-50), and successively outputting to said plural vertical

signal lines the signals which are output from the respective pixels to said horizontal signal lines of plural rows (col. 5, lines 31-36); and horizontal driving means for successively selecting the pixels of plural rows which are selected by said plural systems of vertical driving means (col. 4, lines 59-65). However, Yadid-Pecht does not expressly teach a camera system using as an image pickup device a solid-state image pickup device. Examiner takes Official Notice that it is well known in the art to use a solid-state image pickup device as an image pickup device in a camera system. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yadid-Pecht's solid-state image pickup device with a camera system using as an image pickup device a solid-state image pickup device. This would allow the image sensor of a camera to read the charges in two horizontal lines simultaneously therefore improving the picture quality.

As for **claim 5**, Yadid-Pecht discloses a camera system further comprising a signal processing circuit (fig. 3, ref. 304) containing delay means (fig. 3, ref. SHS) for making signals of plural different rows output from said solid-state image pickup device simultaneous with one another (col. 4, line 66 – col. 5, line 17; col. 5, lines 18-31 and 40-50), and processing means processing the signals of plural rows which are made simultaneous with one another by said delay means (col. 4, line 66 – col. 5, line 17).

11. **Claims 6, 9, and 12-13** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yadid-Pecht et al. (#6,115,065) in view of So (#6,556,244).

For **claim 6**, Yadid-Pecht discloses a solid-state image pickup device (in figs. 2-3) comprising: a pixel portion (fig. 2, ref. 202) in which unit pixels are arranged in a matrix form

(col. 4, lines 41-57); horizontal signal are wired lines of plural rows which said pixel portion on a row basis (col. 4, lines 59-65); a vertical line which is wired commonly to said horizontal signal lines of plural rows (col. 4, lines 59-65); vertical driving means for selecting the pixels of said pixel portion wired to the respective row of said horizontal signal line (col. 5, lines 18-21 and 40-43); and horizontal driving means for selecting pixel of the row selected by said vertical driving means (col. 4, lines 59-65);

Additionally, in fig. 3, Yadid-Pecht discloses pixel comprising a photogate (310), a DC biased transfer gate (311), an output floating diffusion (314), a reset transistor (315), a drain diffusion (316), a gate source follower (317), and a row selection transistor (318). However, he does not expressly disclose a pixel portion wherein said unit pixel comprises a read-out selection transistor for selecting the reading out of the signal charge by a read-out transistor.

In the same field of endeavor, So discloses a pixel portion (in fig. 2) comprising a photoelectric converter (D1) (col. 3, lines 44-46), a read-out transistor (M4) for reading out a signal charge, accumulated by said photoelectric converter (col. 3, lines 59-65), into a storage unit (M5) (col. 3, line 66 – col. 4, lines 5 and 41), a read-out selection transistor (M5) for selecting the reading out of the signal charge by said read-out transistor (col. 4, lines 9-19), an amplifying transistor (M2) for converting the signal charge stored in said storage unit into an electrical signal and for outputting the electrical signal as a pixel signal (col. 3, lines 50-52 and col. 4, lines 53-60), a reset transistor (M1) for resetting the storage unit (col. 3, lines 46-50), and an output selection transistor (M3) for selecting the output of the pixel signal provided by said amplifying transistor (col. 3, lines 52-58). In light of the teachings of So, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yadid-

Pecht's pixel with a read-out selection transistor for selecting the reading out of the signal charge by said read-out transistor, an amplifying transistor for converting the signal charge stored in said storage unit into an electrical signal and for outputting the electrical signal as a pixel signal, and an output selection transistor for selecting the output of the pixel signal provided by said amplifying transistor. This implementation would provide an active pixel sensor (APS) that enables uniform brightness when displayed on a screen (So, col. 2, lines 35-37).

As for **claim 9**, Yadid-Pecht, as modified by So, discloses a solid-state image pickup device wherein said unit pixel outputs a reset level by said reset transistor during a reset operation and a signal level based on the signal charge photoelectrically converted by said photoelectric converter (Yadid-Pecht, col. 4, line 66 – col. 5, line 17). Particularly, in col. 5, lines 9-17, Yadid-Pecht states that in fig. 3 the circuit 304 represents a storage cell shared by a column of active pixels. The storage cell 304 includes a load transistor 320, a first output circuit 321 for buffering and exporting the reset level, and a second output circuit 322 for buffering and exporting the signal level.

As for **claim 12**, Yadid-Pecht, as modified by So, discloses a solid-state image pickup device wherein the device further comprises means for outputting signals of different accumulation time periods (Yadid-Pecht, col. 5, lines 42-50).

As for **claim 13**, Yadid-Pecht discloses a method for driving a solid-state image device pickup device (in figs. 2-3) comprising a pixel portion (fig. 2, ref. 202) having a matrix of unit pixels (col. 4, lines 41-57), each unit pixel comprises a photogate (310), a DC biased transfer gate (311), an output floating diffusion (314), a reset transistor 315, a drain diffusion 316, a gate source follower (317), and a row selection transistor (318).

Yadid-Pecht also discloses horizontal signal lines of plural rows which are wired to said pixel portion on a row basis (col. 4, lines 59-65), a vertical line which is wired commonly to said horizontal signal lines of plural rows (col. 4, lines 59-65), vertical driving means (col. 4, lines 59-65) for selecting the pixels of said pixel portion wired to the respective row of said horizontal signal line (col. 5, lines 18-21 and 40-43), and horizontal driving means for selecting the pixel of the row selected by said vertical driving means (col. 4, lines 59-65).

However, Yadid-Pecht does not expressly disclose a pixel portion wherein said unit pixel comprises a read-out selection transistor for selecting the reading out of the signal charge by said read-out transistor.

Yadid-Pecht also does not expressly disclose a method comprising the steps of: resetting a storage unit by reset transistor; outputting a reset level of said reset transistor to a horizontal signal line through an amplifying transistor; reading out the signal charge of the photoelectric converter into said storage unit; outputting a signal level based on the signal charge to said horizontal signal line through said amplifying transistor; and outputting the reset level and the signal level to a vertical line through said horizontal signal line sequentially.

In the same field of endeavor, So discloses a pixel portion (fig. 2) comprising a photoelectric converter (D1) (col. 3, lines 44-46), a read-out transistor (M4) for reading out a signal charge, accumulated by said photoelectric converter (col. 3, lines 59-65), into a storage unit (M5) (col. 3, line 66 – col. 4, lines 5 and 41), a read-out selection transistor (M5) for selecting the reading out of the signal charge by said read-out transistor (col. 4, lines 9-19), an amplifying transistor (M2) for converting the signal charge stored in said storage unit into an electrical signal and for outputting the electrical signal as a pixel signal (col. 3, lines 50-52 and

col. 4, lines 53-60), a reset transistor (M1) for resetting the storage unit (col. 3, lines 46-50), and an output selection transistor (M3) for selecting the output of the pixel signal provided by said amplifying transistor (col. 3, lines 52-58). So also discloses a method comprising the steps of: resetting a storage unit (M5) by a reset transistor (M5) (col. 4, lines 9-19)*; outputting a reset level of said reset transistor (M5) to a horizontal signal line through an amplifying transistor (55)*; reading out the signal charge of the photoelectric converter into said storage unit (col. 4, lines 1-8); outputting a signal level based on the signal charge to said horizontal signal line through said amplifying transistor (col. 4, lines 1-8); and outputting the reset level and the signal level to a vertical line through said horizontal signal line sequentially (col. 5, lines 9-20).
***Note:** So's transistor (M5) serves as a storage unit and receives reset signals (similarly stated for transistor M2). Please read col. 3, lines 45-50; col. 4, lines 1-19.

In light of the teachings of So, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yadid-Pecht's pixel with a read-out selection transistor for selecting the reading out of the signal charge by said read-out transistor, an amplifying transistor for converting the signal charge stored in said storage unit into an electrical signal and for outputting the electrical signal as a pixel signal, and an output selection transistor for selecting the output of the pixel signal provided by said amplifying transistor. Additionally, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yadid-Pecht's pixel with a method for resetting a storage unit by reset transistor; outputting a reset level of said reset transistor to a horizontal signal line through an amplifying transistor; reading out the signal charge of the photoelectric converter into said storage unit; outputting a signal level based on the signal charge to said horizontal signal line through said

amplifying transistor; and outputting the reset level and the signal level to a vertical line through said horizontal signal line sequentially. These implementations would provide an active pixel sensor (APS) that enables uniform brightness when displayed on a screen (So, col. 2, lines 35-37).

12. **Claims 10-11** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yadid-Pecht et al. (#6,115,065) in view of So (#6,556,244) as applied to claim 6 above, and further in view of Fossum et al. (#5,471,515).

For **claim 10**, Yadid-Pecht, as modified by So, discloses a circuit (Yadid-Pecht, fig. 3, ref. 304) for buffering and exporting both a signal level and a reset level. However, Yadid-Pecht and So do not disclose a solid-state image pickup device wherein the device further comprises a circuit for determining a difference between the reset level and the signal level.

In the same field of endeavor, Fossum discloses disclose a solid-state image pickup device wherein the device further comprises a circuit for determining a difference between the reset level and the signal level. In fig. 3, see VOUTS and VOUTR input to the differential amplifier. Also, read col. 5,lines 9-23. In light of the teachings of Fossum, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yadid-Pecht's imaging device with a circuit for determining a difference between the reset level and the signal level in order to correct for fixed pattern noise by subtracting from it another difference sensed between the two capacitors while they are temporarily shorted (Fossum, col. 2, lines 27-40).

For **claim 11**, Yadid-Pecht, as modified by So and Fossum, discloses a circuit (Yadid-Pecht, fig. 3, ref. 304) for buffering and exporting both a signal level and a reset level. Then, in col. 7, lines 32-38, Yadid-Pecht teaches that one advantage of the destructive readout is that the on-chip correlated doubling sampling can be implemented in many active pixel sensors to suppress noise such as the fixed pattern noise and the kTC noise.

In the same field of endeavor, Fossum teaches that the circuit is a correlated double sampling circuit (col. 4, lines 19-27). In light of the teachings of Fossum, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide Yadid-Pecht's imaging device with a correlated double sampling circuit in order to suppress fixed pattern noise and kTC noise (Fossum, col. 2, lines 35-40).

Allowable Subject Matter

13. **Claims 7-8** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. The following is a statement of reasons for the indication of allowable subject matter:

Claim 7 is allowed because the prior art does not teach or fairly suggest a solid-state image pickup device as claimed in claim 1, wherein said vertical drive means successively output the pixel signals to said vertical line via said horizontal signal line, said horizontal drive means feeds a horizontal selection pulse to said read out selection transistor and said output selection transistor.

Claim 8 is allowed because it is dependent on claim 7.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Egawa et al. (6,801,256)	A CMOS where vertical select lines connected in common to the gates of the individual read transistors of the unit cells in the same rows.
Yonemoto et al. (6,801,253)	An amplifying type solid-state image sensor comprises a photoelectric conversion element, an amplifying element having a storage to store a signal charge transferred thereto from the photoelectric conversion element and serving to convert the signal charge of the storage into an electric signal, and a selector switch for selectively outputting the pixel signal from the amplifying element to a vertical signal line.
Suzuki et al. (6,798,451)	A unit pixel that includes a photodiode as a photoelectric converter, and five N-channel MOS transistors of a read out transistor, a read out selection transistor, an amplifying transistor, a reset transistor, and an output selection transistor.
Tanaka et al. (6,037,577)	An amplifying solid-state image pickup device comprises an image pickup region including photoelectric conversion means, signal charge storage means, signal charge ejection means, row select means, and amplification means, a plurality of vertical select lines arranged in the image pickup region in a row direction, vertical select means for driving the plurality of vertical select lines.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Carramah J. Quiett whose telephone number is (571) 272-7316. The examiner can normally be reached on 8:00-5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber can be reached on (571) 272-7308. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CJQ
May 2, 2005

WENDY R. GARBER
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600